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S3	4	"10055992"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/20 13:44
S4	1	"10/055992"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/20 13:50
S5	26	703/14.ccls. and (voltage same parts)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/20 15:32
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S8	31	703/14.ccls. and (coefficients same voltage)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/20 15:33
S9	4	("5373457" \| "5774382").PN. OR ("6327557").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/07/20 15:44

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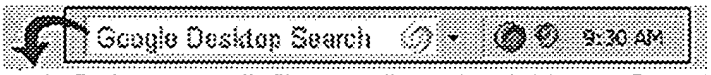
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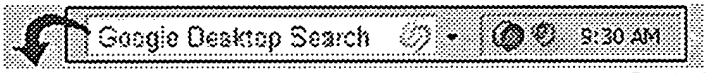
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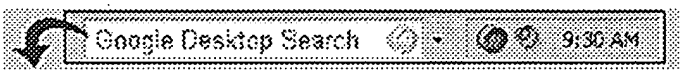
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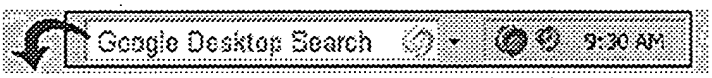
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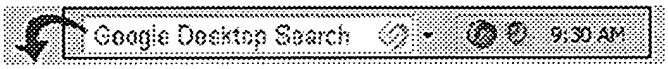
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1 A fast and accurate technique to optimize characterization tables for logic synthesis

John F. Croix, D. F. Wong

June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**

Full text available: pdf(116.00 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Cell characterization data is used by synthesis and timing verificationtools to compile and validate a cell netlist which meets timingconstraints imposed by the designer. Characterization tablescontain data for multiple, simple equations representing a cell's behaviorand are an alternative to the single, monolithic characteristicequation. Data in the table is fit to a function whose form isfixed by the application, and the cellýs response is interpolated fromthe function. Tables can potentially ...

2 Circuit effects in static timing: Osculating Thevenin model for predicting delay and slew of capacitively characterized cells

Bernard N. Sheehan

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(76.62 KB) Additional Information: full citation, abstract, references, index terms

To extrapolate from one point to another using a line, one had better get the slope right. In this paper we apply a similar concept to the important problem in Static Timing Analysis (STA) of predicting cell timing for RC loads using capacitive characterization data. Instead of a line we have a Thevenin circuit, and instead of matching slopes we match load sensitivities. We present a table driven, highly accurate cell delay and slew prediction procedure that can improve STA when interconnect eff ...

Keywords: effective capacitance, static timing analysis

3 Characterization of Boolean functions for rapid matching in FPGA technology mapping

U. Schlichtmann, F. Brglez, M. Hermann

July 1992 **Proceedings of the 29th ACM/IEEE conference on Design automation**

Full text available: pdf(625.19 KB) Additional Information: full citation, references, citings, index terms

4 Automatic generation and characterization of CMOS polycells



C. M. Lee, B. R. Chawla, S. Just

June 1981 **Proceedings of the 18th conference on Design automation**

Full text available: pdf(385.27 KB) Additional Information: full citation, abstract, references, index terms

With increasing complexity and size of integrated circuits, computer aids for layout and simulation have begun to play an ever-increasing role. An approach to take advantage of these aids is the polycell design approach. However, thus far, manual procedures have been used in creating the interior of polycells. A layout style in which CMOS technology lends itself to automation and design rule updatability has been found and is described here. A program has been implemented which takes as inp ...

5 Cell compilation with constraints



Chidchanok Lursinsap, Daniel Gajski

June 1984 **Proceedings of the 21st conference on Design automation**

Full text available: pdf(580.18 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a cell compiler that translates cell descriptions given in form of Boolean equations including pass transistors into layout descriptions in Caltech Intermediate Form (CIF). The translation process is constrained by given height and width of the cell and the position of each I/O signal on the boundary of the cell. Furthermore, the size of each transistor as well as power consumption can be arbitrarily chosen. This cell compiler allows routing through the cell in any dire ...

6 A design rule independent cell compiler



J. S. J. Chen, D. Y. Chen

October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation**

Full text available: pdf(502.84 KB) Additional Information: full citation, abstract, references, index terms

To achieve fast turn around, appropriate performance and efficient silicon area in ASIC design, it is desirable to have the capability of generating new customized cells overnight. A design rule independent cell compiler which is capable of generating nearly optimal layout and all the desirable user interfaces such as automatic place and route database, data sheet, SPICE information and the layout verification mode I for any user specified cell I is reported in this paper. The algorithms us ...

7 Transistor placement for noncomplementary digital VLSI cell synthesis



Michael A. Riepe, Karem A. Sakallah

January 2003 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 8 Issue 1

Full text available: pdf(2.97 MB) Additional Information: full citation, abstract, references, index terms

There is an increasing need in modern VLSI designs for circuits implemented in high-performance logic families such as Cascode Voltage Switch Logic (CVSL), Pass Transistor Logic (PTL), and domino CMOS. Circuits designed in these noncomplementary ratioed logic families can be highly irregular, with complex diffusion sharing and nontrivial routing. Traditional digital cell layout synthesis tools derived from the highly stylized "functional cell" style break down when

confronted with such circuit t ...

Keywords: Cell Synthesis, Euler graphs, benchmark circuits, digital circuits, noncomplementary circuits, sequence pair optimization, transistor chaining, transistor placement

8 Computer-aided design (CAD): A complete methodology for an accurate static noise analysis

Cristiano Forzan, Davide Pandini

April 2005 **Proceedings of the 15th ACM Great Lakes symposium on VLSI**

Full text available: pdf(290.70 KB) Additional Information: full citation, abstract, references, index terms

In signal integrity analysis, the joint effect of propagated noise through library cells, and of the noise injected on a quiet net by neighboring switching nets through coupling capacitances, must be considered in order to accurately estimate the overall noise impact on design functionality and performances.In this work a general macromodel that considers the impact of the cell non-linearity on the noise glitch waveform is proposed, and a new approach that allows to accurately and efficiently mo ...

Keywords: crosstalk, noise propagation, signal integrity

9 Layout synthesis of MOS digital cells

Antun Domic

January 1991 **Proceedings of the 27th ACM/IEEE conference on Design automation**

Full text available: pdf(533.99 KB) Additional Information: full citation, abstract, references, index terms

Synthesis has been used to generate layouts for MOS circuits having a wide range of complexity, from a few to thousands of transistors. Until recently, automatic layout was confined to cell based approaches using a library of pre-laid out cells, such as standard cells or sea-of-gates primitives. The direct use of arbitrary cells, or the quick generation of new library items, is now receiving increased attention. This paper presents an overview of the main issues specific to the cell generat ...

10 Logic and physical CAD: Advanced technology mapping for standard-cell generators

Vinícius Correia, André Reis

September 2004 **Proceedings of the 17th symposium on Integrated circuits and system design**

Full text available: pdf(1.19 MB) Additional Information: full citation, abstract, references, index terms

In this paper, a new algorithm for technology mapping aiming standard-cell generators is proposed. The proposed method has features that explore several AND/OR circuit decompositions by using a n-ary tree representation of the circuit. In the covering step, the cell that leads to the smaller depth increase is chosen. Depth calculation is not limited to the subject tree and takes into account all previously mapped trees representing sub-expressions used as inputs. Experimental results show gains ...

Keywords: cell library, complex gates, library-free, logic synthesis, technology mapping

11 Petri nets as intermediate representation between VHDL and symbolic transition systems
Gert Döhmen
September 1994 **Proceedings of the conference on European design automation**
Full text available: pdf(617.90 KB) Additional Information: full citation, references, citings, index terms

12 An efficient layout style for 2-metal CMOS leaf cells and their automatic generation
Chi-Yi Hwang, Yung-Ching Hsieh, Youn-Long Lin, Yu-Chin Hsu
June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation**
Full text available: pdf(750.81 KB) Additional Information: full citation, references, citings, index terms

13 Delay macromodels for the timing analysis of GaAs DCFL
A. I. Kayssi, K. A. Sakallah
November 1992 **Proceedings of the conference on European design automation**
Full text available: pdf(314.84 KB) Additional Information: full citation, references, index terms

14 SOI Transistor Model for Fast Transient Simulation
D. Nadezhin, S. Gavrilov, A. Glebov, Y. Egorov, V. Zolotov, D. Blaauw, R. Panda, M. Becer, A. Ardelea, A. Patel
November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(164.09 KB) Additional Information: full citation, abstract, index terms

Progress in semiconductor process technology has made SOItransistors one of the most promising candidates for high performanceand low power designs. With smaller diffusion capacitances,SOI transistors switch significantly faster than theirtraditional bulk MOS counterparts and consume less power perswitching. However, design and simulation of SOI MOS circuits ismore challenging due to more complex behavior of an SOI transistorinvolving floating body effects, delay dependence on history oftransist ...

15 Hierarchical constraint transformation using directed interval search for analog system synthesis
Nagu R. Dhanwada, Adrian Nunez-Aldana, Ranga Vemuri
January 1999 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(259.78 KB) Additional Information: full citation, citings, index terms

16 Battery capacity measurement and analysis using lithium coin cell battery
Sung Park, Andreas Savvides, Mani Srivastava
August 2001 **Proceedings of the 2001 international symposium on Low power electronics and design**
Full text available: pdf(313.01 KB) Additional Information: full citation, references, citings, index terms

Keywords: DC/DC converter, battery, coin cell, data acquisition, embedded

system, energy estimation, power estimation

17 Logic transformation for low power synthesis

Ki-Wook Kim, TingTing Hwang, C. L. Liu, Sung-Mo Kang

January 1999 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(140.92 KB) Additional Information: full citation, citings, index terms

18 Technology mapping algorithms for domino logic

Min Zhao, Sachin S. Sapatnekar

April 2002 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 7 Issue 2

Full text available: pdf(480.59 KB) Additional Information: full citation, abstract, references, index terms

We present an efficient algorithm for technology mapping of domino logic to a parameterized library. The algorithm is optimal for mapping trees consisting of two-input AND/OR nodes, and has a computation time that is polynomial in terms of constraint size. The mapping method is then extended to DAG covering that permits the implicit duplication of logic nodes. Our synthesis procedure maps the complementary logic cones independently when AND/OR logic is to be implemented, and together using dual- ...

Keywords: Domino logic, XOR/XNOR logic, dual-monotonic gates, parameterized library, phase assignment, synthesis, technology mapping

19 New ideas in placement: Quantum-Dot Cellular Automata (QCA) circuit partitioning: problem modeling and solutions

Dominic A. Antonelli, Danny Z. Chen, Timothy J. Dysart, Xiaobo S. Hu, Andrew B. Kahng, Peter M. Kogge, Richard C. Murphy, Michael T. Niemier

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(322.29 KB) Additional Information: full citation, abstract, references, index terms

This paper presents the Quantum-Dot Cellular Automata (QCA) physical design problem, in the context of the VLSI physical design problem. The problem is divided into three subproblems: partitioning, placement, and routing of QCA circuits. This paper presents an ILP formulation and heuristic solution to the partitioning problem, and compares the two sets of results. Additionally, we compare a human-generated circuit to the ILP and Heuristic solutions. The results demonstrate that the heuristic is ...

Keywords: circuit partitioning, computer aided design, quantum-dot cellular automata (QCA)

20 Iterative realization of multivalued logic systems

Vason P. Srini

January 1978 **Proceedings of the eighth international symposium on Multiple-valued logic**

Full text available: pdf(438.47 KB) Additional Information: full citation, abstract, references, index terms

The realization of multivalued combinational functions and sequential machines by using arrays of one type of cells is considered. The algebra used for the multivalued logic system has two binary operations and a set of unary operations. Each of these operations is realized by a cellular array. The cells are combinational

and implemented by using binary logic gates. The cells are also designed so that all unrestricted multiple faults in arrays of these cells are detectable. Multivalued comb ...

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1 A power modeling and characterization method for the CMOS standard cell library

Jiing-Yuan Lin, Wen-Zen Shen, Jing-Yang Jou

January 1997 **Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(86.12 KB) Publisher Site Additional Information: full citation, abstract, references, index terms

In this paper, we propose power consumption models for complex gates and transmission gates, which are extended from the model of basic gates proposed in [1]. We also describe an accurate power characterization method for CMOS standard cell libraries which accounts for the effects of input slew rate, output loading, and logic state dependencies. The characterization methodology separates the power consumption of a cell into three components, e.g., capacitive feedthrough power, short-circuit powe ...

Keywords: power characterization, power estimation, power consumption

2 Interconnect: Thermal aware cell-based full-chip electromigration reliability analysis

Syed M. Alam, Donald E. Troxel, Carl V. Thompson

April 2005 **Proceedings of the 15th ACM Great Lakes symposium on VLSI**

Full text available: pdf(356.26 KB) Additional Information: full citation, abstract, references, index terms

A hierarchical scheme with cells and modules is crucial for managing design complexity during a large integrated circuit design. We present a methodology for thermal aware cell-based electromigration analysis suitable for integrating electromigration reliability analysis into a conventional IC design flow. A block or cell is characterized for reliability while it is characterized for power and timing. Reusing cell characterization data significantly reduces computational load while analyzing a f ...

Keywords: IC thermal analysis, electromigration, full-chip reliability, reliability aware design, reliability characterization

3 Power estimation of cell-based CMOS circuits
Alessandro Bogiolo, Luca Benini, Bruno Riccò
June 1996 **Proceedings of the 33rd annual conference on Design automation**
Full text available: pdf(218.93 KB) Additional Information: full citation, references, citings, index terms

4 Modeling and simulation of the interference due to digital switching in mixed-signal ICs
Alper Demir, Peter Feldmann
November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(209.73 KB) Additional Information: full citation, abstract, references, citings, index terms

The paper introduces a methodology for the evaluation of the interference noise, caused by digital switching activity, in sensitive circuits of a mixed-digital-analog chip. The digital switching activity is modeled stochastically as functions defined on Markov chains. The actual interference signal is obtained through the modulation of this discrete stochastic signal with real current injection patterns stored a priori in a pre-characterized library. The interference noise results from the ...

5 Numerical techniques for simulation: High-level simulation of substrate noise in high-ohmic substrates with interconnect and supply effects
G. Van der Plas, M. Badaroglu, G. Vandersteen, P. Dobrovolny, P. Wambacq, S. Donnay, G. Gielen, H. De Man
June 2004 **Proceedings of the 41st annual conference on Design automation**
Full text available: pdf(509.42 KB) Additional Information: full citation, abstract, references, index terms

Substrate noise is a major obstacle for mixed-signal integration. In this paper we propose a fast and accurate high-level methodology to simulate substrate noise generated by large digital circuits. The methodology can handle any substrate type, e.g. bulk-type or EPI-type, and takes into account the effects of interconnect and supply. For each standard cell a substrate macromodel is used in order to efficiently simulate the total system, which consists of a network of such macromodels. For a ...

***Keywords**: model order reduction, modeling, substrate noise*

6 Automatic import of custom designs into a cell-based environment using switch-level analysis and circuit simulation
Ronald Stewart, Véronique Anjubault, Philippe Garcin, Jacques Benkoski
November 1992 **Proceedings of the conference on European design automation**
Full text available: pdf(406.13 KB) Additional Information: full citation, references, index terms

7 Accurate and efficient macromodel of submicron digital standard cells
Cristiano Forzan, Bruno Franzini, Carlo Guardiani
June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**
Full text available: pdf(76.45 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

In this paper a new analytic gate delay modelingtechnique is presented that allows to accuratelyreproduce the timing behavior of deep submicron digitalstandard cells for a large range of operating conditions.The proposed technique sensibly improves the accuracyof the existing analytic delay models and it usuallyrequires less simulations for the cell characterization.Moreover it is compatible with the most advanced interconnectdelay models that have been recently proposed inthe literature.

8 Poster session 2: Design and characterization of an and-or-inverter (AOI) gate for QCA implementation

Jing Huang, Mariam Momenzadeh, Mehdi B. Tahoori, Fabrizio Lombardi

April 2004 **Proceedings of the 14th ACM Great Lakes symposium on VLSI**

Full text available: pdf(178.57 KB) Additional Information: full citation, abstract, references, index terms

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Keywords: QCA, defect characterization, test

9 Particle-in-cell simulation codes in High Performance Fortran

Erol Akarsu, Kivanc Dincer, Tomasz Haupt, Geoffrey C. Fox

November 1996 **Proceedings of the 1996 ACM/IEEE conference on Supercomputing (CDROM) - Volume 00**

Full text available: pdf(316.89 KB) Additional Information: full citation, abstract, references, citings, index terms

Particle-in-Cell (PIC) plasma simulation codes model the interaction of charged particles with surrounding electrostatic and magnetic fields. Its computational requirements made it to be classified as one of the grand-challenge problems facing the high performance community. In this paper we present the implementation of 1-D and 2-D electrostatic PIC codes in High Performance Fortran(HPF) on a IBM SP-2. HPF expands Fortran 90 with data distribution and alignment directives and data parallel ...

Keywords: Particle-in-Cell, High Performance Fortran

10 SOI Transistor Model for Fast Transient Simulation

D. Nadezhin, S. Gavrilov, A. Glebov, Y. Egorov, V. Zolotov, D. Blaauw, R. Panda, M. Becer, A. Ardelea, A. Patel

November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(164.09 KB) Additional Information: full citation, abstract, index terms

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11 Advances in accelerated simulation: Circuit-aware architectural simulation

Seokwoo Lee, Shidhartha Das, Valeria Bertacco, Todd Austin, David Blaauw, Trevor Mudge

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(291.91 KB) Additional Information: full citation, abstract, references, citings, index terms

Architectural simulation has achieved a prominent role in the system design cycle by providing designers the ability to quickly examine a wide variety of design choices. However, the recent trend in system design toward architectures that react to circuit-level phenomena has outstripped the capabilities of traditional cycle-based architectural simulators. In this paper, we present an architectural simulator design that incorporates a circuit modeling capability, permitting architectural-level si ...

Keywords: architectural simulation, circuit simulation, computer system simulation, high-performance simulation

12 Characterization of user mobility in low earth orbit mobile satellite systems

Enrico Del Re, Romano Fantacci, Giovanni Giambene

May 2000 **Wireless Networks**, Volume 6 Issue 3

Full text available: pdf(422.15 KB) Additional Information: full citation, abstract, references, index terms

Future mobile communication networks will provide a global coverage by means of constellations with nongeosynchronous satellites. Multi‐spot‐beam antennas on satellites will allow a cellular coverage all over the Earth. Due to the unstationarity of satellites a call may require many cell changes during its lifetime. These passages will be managed by inter‐beam handover procedures. This paper deals with the modeling of the user cell change process during call lifetime in Low E ...

13 Manufacturing applications: A basic study on autonomous characterization of square array machining cells for agile manufacturing

Susumu Fujii, Hiroshi Morita, Takeshi Tanaka

December 2000 **Proceedings of the 32nd conference on Winter simulation**

Full text available: pdf(313.91 KB) Additional Information: full citation, abstract, references

In this study, a manufacturing system locating machining cells in a square array is considered as an agile manufacturing system that can manufacture a variety of kinds of products with varying volumes. Each cell can process any work whose machining operations for each work are divided into some operation groups common to all works. An auction-based algorithm is proposed to select a cell to process a work after its processing of one operation group. Five types of bid are considered and their effe ...

14 Analysis of performance impact caused by power supply noise in deep submicron devices

Yi-Min Jiang, Kwang-Ting Cheng

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

Full text available: pdf(153.12 KB) Additional Information: full citation, references, citings, index terms

15 MAELSTROM: efficient simulation-based synthesis for custom analog cells
Michael Krasnicki, Rodney Phelps, Rob A. Rutenbar, L. Richard Carley
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Full text available: pdf(129.41 KB) Additional Information: full citation, references, citings, index terms

16 Circuit effects in static timing: Osculating Thevenin model for predicting delay and slew of capacitively characterized cells
Bernard N. Sheehan
June 2002 **Proceedings of the 39th conference on Design automation**
Full text available: pdf(76.62 KB) Additional Information: full citation, abstract, references, index terms

To extrapolate from one point to another using a line, one had better get the slope right. In this paper we apply a similar concept to the important problem in Static Timing Analysis (STA) of predicting cell timing for RC loads using capacitive characterization data. Instead of a line we have a Thevenin circuit, and instead of matching slopes we match load sensitivities. We present a table driven, highly accurate cell delay and slew prediction procedure that can improve STA when interconnect eff ...

Keywords: effective capacitance, static timing analysis

17 Session 6D: Analog synthesis: ASF: a practical simulation-based methodology for the synthesis of custom analog circuits
Michael J. Krasnicki, Rodney Phelps, James R. Hellums, Mark McClung, Rob A. Rutenbar, L. Richard Carley
November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(225.63 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes ASF, a novel cell-level analog synthesis framework that can size and bias a given circuit topology subject to a set of performance objectives and a manufacturing process. To manage complexity and time-to-market, SoC designs require a high level of automation and reuse. Digital methodologies are inapplicable to analog IP, which relies on tight control of low-level device and circuit properties that vary widely across manufacturing processes. This analog synthesis solution aut ...

18 PASTEL: a parameterized memory characterization system
K. Ogawa, M. Kohno, F. Kitamura
February 1998 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(210.31 KB) Additional Information: full citation, abstract, references, citings, index terms
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PASTEL is a parameterized memory characterization system which extracts the characteristics of ASIC on-chip-memories such as delay, timing and power consumption which are important in LSI logic design. PASTEL is a fully-automated process from exact wire-RC extraction through circuit reduction, input vector generation, waveform measurement, data-sheet and library creation. The circuit reduction scheme can reduce the circuit simulation time by 2 order of magnitude while maintaining delay error wit ...

Keywords: automatic characterization, on-chip-memory, timing, power, cell

library, LSI, ASIC

19 A comparative study of fuzzy versus "fixed" thresholds for robust queue management in cell-switching networks
Allen R. Bonde, Sumit Ghosh
August 1994 **IEEE/ACM Transactions on Networking (TON)**, Volume 2 Issue 4
Full text available: pdf(976.98 KB) Additional Information: full citation, references, citings, index terms

20 Toward a Formal Theory of Modeling and Simulation: Structure Preserving Morphisms
Bernard P. Zeigler
October 1972 **Journal of the ACM (JACM)**, Volume 19 Issue 4
Full text available: pdf(1.39 MB) Additional Information: full citation, references, citings, index terms

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1 A power modeling and characterization method for the CMOS standard cell library

Jiing-Yuan Lin, Wen-Zen Shen, Jing-Yang Jou

January 1997 **Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(86.12 KB) Publisher Site Additional Information: full citation, abstract, references, index terms

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Keywords: power characterization, power estimation, power consumption

2 Manufacturing applications: A basic study on autonomous characterization of square array machining cells for agile manufacturing

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3 Characterization of user mobility in low earth orbit mobile satellite systems

Enrico Del Re, Romano Fantacci, Giovanni Giambene

May 2000 **Wireless Networks**, Volume 6 Issue 3

Full text available: pdf(422.15 KB) Additional Information: full citation, abstract, references, index terms

Future mobile communication networks will provide a global coverage by means of constellations with nongeosynchronous satellites. Multi‐spot‐beam antennas on satellites will allow a cellular coverage all over the Earth. Due to the unstationarity of satellites a call may require many cell changes during its lifetime. These passages will be managed by inter‐beam handover procedures. This paper deals with the modeling of the user cell change process during call lifetime in Low E ...

4 A fast and accurate technique to optimize characterization tables for logic synthesis

John F. Croix, D. F. Wong

June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**

Full text available: pdf(116.00 KB) Additional Information: full citation, abstract, references, citings, index terms
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Cell characterization data is used by synthesis and timing verificationtools to compile and validate a cell netlist which meets timingconstraints imposed by the designer. Characterization tablescontain data for multiple, simple equations representing a cell's behaviorand are an alternative to the single, monolithic characteristicequation. Data in the table is fit to a function whose form isfixed by the application, and the cellýs response is interpolated fromthe function. Tables can potentially ...

5 Interconnect: Thermal aware cell-based full-chip electromigration reliability analysis

Syed M. Alam, Donald E. Troxel, Carl V. Thompson

April 2005 **Proceedings of the 15th ACM Great Lakes symposium on VLSI**

Full text available: pdf(356.26 KB) Additional Information: full citation, abstract, references, index terms

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Keywords: IC thermal analysis, electromigration, full-chip reliability, reliability aware design, reliability characterization

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Bernard N. Sheehan

June 2002 **Proceedings of the 39th conference on Design automation**

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Keywords: effective capacitance, static timing analysis

7 A homogeneous PCS network with markov call arrival process and phase type cell residence time
Attahiru Sule Alfa, Wei Li
November 2002 **Wireless Networks**, Volume 8 Issue 6
Full text available: pdf(163.25 KB) Additional Information: full citation, abstract, references, index terms

In this paper, the arrival of calls (i.e., new and handoff calls) in a personal communications services (PCS) network is modeled by a Markov arrival process (MAP) in which we allow correlation of the interarrival times among new calls, among handoff calls, as well as between these two kinds of calls. The PCS network consists of homogeneous cells and each cell consists of a finite number of channels. Under the conditions that both cell's residence time and the requested call holding time possess ...

Keywords: duration of call blocking period, markovian arrival process (MAP), personal communications services (PCS) network model, phase type (PH) distribution

8 Automatic import of custom designs into a cell-based environment using switch-level analysis and circuit simulation
Ronald Stewart, Véronique Anjubault, Philippe Garcin, Jacques Benkoski
November 1992 **Proceedings of the conference on European design automation**
Full text available: pdf(406.13 KB) Additional Information: full citation, references, index terms

9 The SPLASH-2 programs: characterization and methodological considerations
Steven Cameron Woo, Moriyoshi Ohara, Evan Torrie, Jaswinder Pal Singh, Anoop Gupta
May 1995 **ACM SIGARCH Computer Architecture News , Proceedings of the 22nd annual international symposium on Computer architecture**, Volume 23 Issue 2
Full text available: pdf(1.73 MB) Additional Information: full citation, abstract, references, citings, index terms

The SPLASH-2 suite of parallel applications has recently been released to facilitate the study of centralized and distributed shared-address-space multiprocessors. In this context, this paper has two goals. One is to quantitatively characterize the SPLASH-2 programs in terms of fundamental properties and architectural interactions that are important to understand them well. The properties we study include the computational load balance, communication to computation ratio and traffic needs, impor ...

10 Characterization of Boolean functions for rapid matching in FPGA technology mapping
U. Schlichtmann, F. Brglez, M. Hermann
July 1992 **Proceedings of the 29th ACM/IEEE conference on Design automation**
Full text available: pdf(625.19 KB) Additional Information: full citation, references, citings, index terms

11 Delay and noise modeling in the nanometer regime: Blade and razor: cell and interconnect delay analysis using current-based models

John F. Croix, D. F. Wong

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(246.93 KB) Additional Information: full citation, abstract, references, citings, index terms

In order to adequately account for nanometer effects during timing analysis, archaic standard cell models must be replaced. Simplifying assumptions used during characterization, such as nearly linear voltage inputs or lumped-capacitance loads, are no longer valid. Signal integrity analysis further complicates the characterization process because the typical voltage waveform used during characterization does not contain a noise component. This paper introduces two new technologies for standard ce ...

Keywords: blade, cell model, current-based model, interconnect model, razor, recursive convolution, timing analysis

12 Power estimation of cell-based CMOS circuits

Alessandro Bogiolo, Luca Benini, Bruno Riccò

June 1996 **Proceedings of the 33rd annual conference on Design automation**

Full text available: pdf(218.93 KB) Additional Information: full citation, references, citings, index terms

13 Poster session 2: Design and characterization of an and-or-inverter (AOI) gate for QCA implementation

Jing Huang, Mariam Momenzadeh, Mehdi B. Tahoori, Fabrizio Lombardi

April 2004 **Proceedings of the 14th ACM Great Lakes symposium on VLSI**

Full text available: pdf(178.57 KB) Additional Information: full citation, abstract, references, index terms

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Keywords: QCA, defect characterization, test

14 Automatic generation and characterization of CMOS polycells

C. M. Lee, B. R. Chawla, S. Just

June 1981 **Proceedings of the 18th conference on Design automation**

Full text available: pdf(385.27 KB) Additional Information: full citation, abstract, references, index terms

With increasing complexity and size of integrated circuits, computer aids for layout and simulation have begun to play an ever-increasing role. An approach to take advantage of these aids is the polycell design approach. However, thus far, manual procedures have been used in creating the interior of polycells. A layout style in which CMOS technology lends itself to automation and design rule updatability has been found and is described here. A program has been implemented which takes as inp ...

15 LCS—a leaf cell synthesizer employing formal deduction techniques

P. A. Subrahmanyam

October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation**

Full text available: pdf(1.02 MB) Additional Information: full citation, abstract, references, index terms

This paper discusses the use of formal reasoning techniques to aid in the automated structural design of leaf cells, in the more global context of VLSI circuit design. The technique supports an encapsulation of the technology-dependent aspects of a design by using appropriate formal models, and guarantees the consistency of the designs produced with respect to the functional specification and the technology model employed. The approach is illustrated by its use in the design of some leaf ce ...

16 PASTEL: a parameterized memory characterization system

K. Ogawa, M. Kohno, F. Kitamura

February 1998 **Proceedings of the conference on Design, automation and test in Europe**

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Keywords: automatic characterization, on-chip-memory, timing, power, cell library, LSI, ASIC

17 A power modeling and characterization method for macrocells using structure information

Jing-Yuan Lin, Wen-Zen Shen, Jing-Yang Jou

November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**

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To characterize a macrocell, a general method is to store the power consumption of all possible transition events at primary inputs in the lookup tables. Though this approach is very accurate, the lookup tables could be huge for the macrocells with many inputs. In this paper, we present a new power modeling method which takes advantage of the structure information of macrocells and selects minimum number of primary inputs or internal nodes in a macrocell as state variables to build a state trans ...

Keywords: Power modeling for macrocells, RTL power estimations, State transition graph, and Power characterization.

18 Characterization of VAX Macsyma

John K. Foderaro, Richard J. Fateman

August 1981 **Proceedings of the fourth ACM symposium on Symbolic and algebraic computation**

Full text available: pdf(531.17 KB) Additional Information: full citation, abstract, references, citings, index terms

The algebraic manipulation system Macsyma [Grou77, Fate80] has been running for over a year on Digital Equipment Corp. VAX-11 large-address-space medium-scale computers [Stre78]. In order to run Macsyma in this environment, a Lisp system for the VAX, FRANZ LISP[Fode50], was constructed at Berkeley. The goal of running Macsyma provided direction and motivation and is partially responsible for the rapid development of the Lisp system. Because Lisp is a high level language there are ...

19 Iterative tree automata, alternating Turing machines, and uniform Boolean circuits: relationships and characterization

Abdelaziz Fellah, Sheng Yu

March 1992 **Proceedings of the 1992 ACM/SIGAPP symposium on Applied computing: technological challenges of the 1990's**

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20 Poster papers: Tumor cell identification using features rules

Bin Fang, Wynne Hsu, Mong Li Lee

July 2002 **Proceedings of the eighth ACM SIGKDD international conference on Knowledge discovery and data mining**

Full text available: pdf(152.89 KB) Additional Information: full citation, abstract, references, citings, index terms

Advances in imaging techniques have led to large repositories of images. There is an increasing demand for automated systems that can analyze complex medical images and extract meaningful information for mining patterns. Here, we describe a real-life image mining application to the problem of tumour cell counting. The quantitative analysis of tumour cells is fundamental to characterizing the activity of tumour cells. Existing approaches are mostly manual, time-consuming and subjective. Efforts t ...

Keywords: dynamic water immersion, features rules, identification, local adaptive thresholding, majority vote, meta classifier, weighted vote

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